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CWS

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WaveIntegrity™ from CWS Used by STMicroelectronics for Early Noise Analysis in CMOS and FD-SOI SoCs

EDA tool ensures rapid and practical analysis of noise issues in complex SoCs

Crolles, France/September 15 th,2014 –Today’s SoCs, with their mixture of multiple digital and analog blocks, are often subject to issues and unnecessary constraints, as design teams seek to avoid potential noise-related problems. CWS today announced that STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronics applications, is using WaveIntegrity™ tools to help ST remove the risks caused by on-chip, package, and PCB noise parasitics.

Following evaluation across multiple projects covering both CMOS and FD-SOI processes, ST is using WaveIntegrity™ across groups designing complex IP for Home and Automotive devices. Getting a fast, initial picture of potential noise-related issues is vital in designing today’s complex SoCs and WaveIntegrity performs noise-analysis results right from the initial floorplan, as IPs are delivered to the chip assembly team.

WaveIntegrity encourages noise-analysis results to be used during the first and subsequent floorplan stages, so that critical design decisions can be made early and at low cost. The analysis setup is then refined for the final floorplan revision to support any potential remaining noise-related design choices before final chip P&R.

“The complexity, frequency and increasingly stringent power requirements of SoC designs increase year-on-year. Successfully verifying the noise characteristics of the SoCs, the package they are placed in, and the PCBs they are inserted on, has become an increasingly difficult challenge: applying “rules of thumb” is no longer adequate. WaveIntegrity™ supports such analysis, and enables verification previously considered impractical by other means,” commented Brieuc Turluche, president and CEO of CWS. “With multiple teams contributing to each design it is essential that noise analysis is both easy and rapid to implement at each stage. Deployment by ST is a proof-point for CWS.”

“ST needed a fast, practical method to ensure our IP would not be susceptible to noise issues, when implemented in complex, multi-million gate SoCs. We have also found we can optimize the power-supply requirements to IP in the knowledge that both the position and number of pins or bumps will be adequate for the IP as implemented,” said Pierre Dautriche, Physical IP & Mixed Design Solutions Director, Central CAD & Design Solutions, STMicroelectronics. “Extensive use here has proven WaveIntegrity™ as the most efficient and effective way to achieve these aims, allowing us to reduce risk in ways previously impossible. This capability is being extended to both our most advanced and older process nodes, and which we will also support for our own customers. ”

To learn more visit www.cwseda.com

About CWS

CWS enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use CWS software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in 196C, Rue du Rocher de LORZIER, F-38430, Moirans, France. More information about the company, its products, and services is available at www.cwseda.com.

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