CWS Launches SiPEX, a Productivity Tool for RF SOI Designs

SiPEX shrinks the time-to-market for fabless companies using RF SOI-processes through fast and automated simulation, and by closing the gap between simulation and silicon measurements

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PARIS & SAN JOSE, Calif.--(BUSINESS WIRE)--Coupling Wave Solutions, S.A. (CWS), a leader in solutions for interference analysis in complex chip designs incorporating RF and analog blocks, today announced the availability of a new productivity tool called SiPEX. SiPEX models the silicon substrate on insulators much faster than any other tools in its class and allows radio frequency (RF) silicon-on-insulator (SOI) designers to increase the number of design iterations—including Spice simulation—up to 10 times in the same time frame.

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"We are delighted to make this product available to our customers. By allowing an RF switch designer to make ten times more design iterations per day, we are increasing their productivity at a reduced cost-of-ownership. With SiPEX, RF switch designers will be able to make their design changes in less than 15 minutes and obtain a few decibels (dB) of variation over silicon measurements in simulation. This is a dramatic improvement over current productivity levels," said Brieuc Turluche, chairman of the board of directors and chief executive officer of CWS.

"State-of-the-art RF front-end components require advanced design methodologies and tools. SiPEX helped us improve our productivity and close the gap between simulation and silicon measurements when optimizing the linearity of our chips," said *Greg Caltabiano*, CEO of *ACCO,* a fabless semiconductor company developing innovative highly integrated semiconductor solutions for the Internet of Things (IoT) and the Smart Phone RF Front End.

With SiPEX, RF designers can either evaluate more design implementations in any given time frame, or accelerate the tape out to the RF SOI foundry, shortening the time-to-market. SiPEX provides field solver-like accuracy. In addition, RF SOI foundry can back-annotate the silicon measurements in their Process Design Kit (PDK) and ensure that Spice simulation with SiPEX will match the actual silicon measurements.

SiPEX is available as a plug-in for generic interconnect parasitic extraction tools including Mentor Graphic's Calibre®.

About CWS

CWS is the leading provider of parasitic extraction and activity modeling tools for system-level interference analysis of complex designs incorporating RF and analog blocks, targeting SOI applications or advanced bulk process nodes including 28nm and below. CWS unique harmonic analysis approach allows for controlling and managing noise issues throughout the design cycle from components, to packages, up to and including board design. Wrapped in 'easy-to-deploy' software bundle, WaveIntegrity™ is used by chip architects and designers to drive the chip design floorplanning and by package and PCB designers to integrate the noise-related design constraints in the final chip operational environment. Founded in 2003, CWS' offices are located in Paris, Grenoble, France and San Jose, USA. More information about the company, its products, and services is available at www.cwseda.com.

Contacts

For Coupling Wave Solutions, S.A.
Brieuc Turluche, +33 (0) 4-76-35-80-09
contact@cwseda.com
or
Public Relations
Barbara Rizzatti, +1-971-998-9404