Press Release

Minalogic Presents 11 Cutting-Edge French Companies and Labs at the Design Automation Conference in San Francisco

Grenoble, France and San Francisco, California - June 1, 2015 - Minalogic, the French innovation cluster dedicated to smart systems integration and digital solutions, will accompany 9 innovative French companies and 2 labs at the Design Automation Conference (DAC), the USA's premier conference for design and automation of electronic systems. The French delegation of companies includes Asygn, CWS, DeFacTo Technologies, Docea Power, EdXact, InfiniScale, Iroc Technologies, Magillem and Xyalis, as well as the CEA Tech Leti and CMP labs.

During the 5 days of the conference, which runs from June 7 to 11, Minalogic will showcase the breadth and depth of skills of the electronic design automation (EDA) companies based in the Grenoble-Isère area of France. In addition, the cluster will promote the numerous existing synergies and mutually beneficial long-term partnerships established between the companies and the local R&D labs over the last 10 years, since the foundation of Minalogic in 2005.

Ranked as one of the 5 most inventive cities in the world (Forbes 2013), Grenoble is one of the premier locations for EDA across the globe. With industry leaders like ARM, Atrenta, Mentor Graphics and Synopsys, the region encompasses each link of the EDA value chain: from design to development to equipment manufacturing, as well as cleanroom environments and related services. Moreover, the companies and R&D labs in Grenoble benefit from the proximity to major manufacturers (STMicroelectronics, Soitec, e2V) and world's top universities.
With over 25,000 jobs and 1,200 graduates in the field of micro-nanotechnologies & electronics, the region benefits from a unique culture of collaboration between R&D, academia and industry.
By fostering collaboration and open innovation, the Minalogic cluster contributes to the realization of the great innovation potential of the French EDA companies.

Press Invitation:
Monday June 8th, from 4:00 to 6:00 pm - W Hotel, 181 3rd St, San Francisco
Together with AEPI (the Grenoble-Isère Economic Development Agency) and CEA-Leti, Minalogic is honored to invite you to a **Networking Event bringing together the Grenoble delegation and other EDA industry leaders attending DAC.**
During the event, **Philippe Magarshack**, President of Minalogic and CTO Embedded Processing Solutions at STMicroelectronics, will introduce the cluster highlighting its key competitive advantages.
Dr. Jan Rabaey, Donald O. Pederson Distinguished Professorship at UC Berkeley, will deliver a speech on "Design Trends and EDA Challenges, from Connected Objects to Cloud Computing".
The participants will celebrate the launch of **Silicon Impulse**, the new IC design competence center hosted by CEA-Leti in Grenoble. This center is entirely dedicated to Designing innovative Silicon Products based on disruptive innovation, such as FD-SOI, which are led by major industry leaders based in the Grenoble region.

RSVP required *http://www2.minatec.com/aepi_DAC2015/survey.htm*

For any questions and interview booking, please contact onsite:
Erasmia Dupenloup, Director, Business Development, +33 6 45 59 10 57

French companies and labs at DAC 2015:

- **ASYGN**

  ASYGN serves MEMS, imaging and RF industries providing specific IPs, design services and tools. ASYGN tools and methodology focus on automating mixed-signal systems functional verification procedures all along the design cycle.

  Recent releases from ASYGN include low-power image sensor chips, circuits for High performance Mems-based Inertial Measurement Units, and gas sensors interfaces.

  http://www.asygn.com

- **CEA Tech Leti,** *booth 1207*

  Leti, in partnership with the GRENOBLE (France) semiconductor eco-system is launching Silicon Impulse™, a new initiative around FDSOI ICs design and fabrication.

  We aim at facilitating the access to these new technologies (28 nm Ultra Low Power and high performance SOCs and related Innovative IPs) for IC design teams through Industrial quality MPW vehicles, prototyping and production of pre-series.

  We benefit from the experience of our design team at Leti that has gained knowledge through the design and prototyping of various circuits over the past 4 or 5 years. Our track record includes the implementation of a wide I/O memory chip in 2012, the design and fabrication of a high performance low power DSP core, the prototyping of various designs for embedded memories functions as well as specific architectures for mmW front-ends.

  http://www.leti.fr/en

- **CMP,** *booth 2217*

  CMP is a service organization in ICs and MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial companies.

  Advanced industrial technologies are available in CMOS, SiGe BiCMOS, HV-CMOS, SOI, P-HEMT GaAs, MEMS, 3D-IC, etc. CMP distributes and supports several CAD software tools for both Industrial Companies and Universities.

  Since 1981, more than 1000 Institutions from 70 countries have been served, more than 6700 projects have been prototyped through 800 runs, and 60 different technologies have been interfaced.

  http://cmp.imag.fr

- **CWS**

  CWS : Coupling Wave Solutions® (CWS) innovative software helps IP block authors and system integrators to successfully incorporate analog and RF IP blocks on complex system on chips (SOCs) where rapid and/or large variations of electrical signals, such as the switching activities in digital data processing, present a highly hostile environment.

  WaveIntegrity™ aims at modeling noise generation and propagation through the combination of substrate, interconnect and package magneto-static parasitic, and allows for system-level noise analysis very early in the design cycle.

  http://www.cwseda.com

- **DEFACTO TECHNOLOGIES,** *booth 1902*

  Defacto Technologies is an innovative chip design software company providing breakthrough RTL platforms to enhance IP Integration, Design Verification & RTL Signoff of IP cores and System on Chips. Defacto EDA solutions help solve design problems in different areas such as SoC integration, low power, clock verification, RTL signoff, ECO and DFT.

  http://www.defactotech.com

- **DOCEA POWER,** *booth 3507*

  Docea Power provides software solutions to model and simulate the power consumption and thermal behavior of electronic systems from an architectural perspective. The solutions are used to secure specifications, optimize the power behavior and accelerate the validation and verification of design projects. Docea Power solutions apply to both electronic systems (board, OEM devices) and semiconductor devices (IC, SoC, System in Package).

  http://www.edxact.com

- **EdXact,** *booth 2915*

  EdXact focuses on design tools aimed at physical design and verification of Integrated Circuits, with a specialization on questions related to netlist parasitics and their impact on simulation time, signal integrity, delay, crosstalk and other. EdXact is best known for netlist reduction technology JIVARO, offering additional dedicated analysis tools BELLEDONNE and VISO.
  http://www.edxact.com

- **InfiniScale,** *booth 510*

  InfiniScale is a leading provider of innovative software solutions that address Analog & RF, IO and Memory process variability challenges and parametric yield optimization at aggressive technologies. At DAC 2015, Infiniscale introduces a new release of ICLys, a major technology breakthrough that provides a robust accurate High-Sigma analyzer and a unique Fast Monte Carlo simulation that speeds up Brute Monte Carlo (MC) up to 30X+ while guaranteeing an equivalent accuracy.
  http://www.infiniscale.com

- **IROC Technologies,** *booth 2123*

  IROC Technologies is a private company established in 2000 in Grenoble, France. IROC offers Test services, aiming at validating and qualifying device reliability through physical experiments; EDA tools, aiming at predicting devices sensitivity to perturbations; Design solutions and services, aiming at hardening devices to external and internal perturbations. IROC is offering its services and products to leaders of the electronic business, from foundries to system houses.
  http://www.iroctech.com

- **Magillem,** *booth 2414*

  Magillem, is a leading provider of front-end design xml solutions and best-in-class tools to reduce the global cost of complex designs and assist companies with their core business.Vision is ISDD ™, i.e. Integrated Specification, Design & Documentation, the new paradigm in SoC design. Magillem will present a cutting edge virtual platform technology for IoT systems at DAC 2015
  http://www.magillem.com

- **XYALIS,** *booth 2606*

  XYALIS offers specialized tools in the area of Design for Manufacturing. XYALIS main tools includes CMP metal fill and MPW or shuttle layout optimization.
  At DAC 2015, XYALIS introduces WISC, a collaborative web-based Multi Project Wafer (MPW) graphical editor which automates requests, handles approval processes, secures data exchanges between shuttle Mask Data Preparation teams and contributors design teams.
  http://www.xyalis.com

 With the support of the Rhone-Alpes Region (France)

About Minalogic
Created in 2005 and based in Rhone-Alpes (France), the Minalogic global innovation cluster is a public/private partnership with 300 members dedicated to smart systems integration and digital solutions.
Minalogic's collaborative projects are focused on developing products and services that capitalize on the potential of better combinations of micro- and nanoelectronics, photonics and software. Nearly 400 projects have been certified and financed, with a total R&D spending of €2 billion.
The cluster encourages and supports industry research-training collaborations with companies in Europe, Asia and the U.S., while responding to the global high-tech community's need to identify new value-added services that can be integrated into existing products in the fields of ICT, healthcare, energy, construction, advanced manufacturing, transportation and sports & outdoors.

Further information on www.minalogic.com - Follow Minalogic on twitter.com/Minalogic_EN

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