CWS SiPEX Released in TowerJazz's CS18 (RF SOI) Process Design Kits

The new design tool improves the linearity of RF designs and accurately simulate and model critical RF functions for 5G and IoT communications

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PARIS -- Coupling Wave Solutions, S.A. (CWS), a leader in solutions for interference analysis in complex chip designs incorporating RF and analog blocks, today announced TowerJazz (NASDAQ: TSEM), the global specialty foundry leader, has adopted CWS' SiPEX in its CS18 RF SOI process design kits (PDKs) to provide improved substrate modeling. SiPEX models the silicon substrate on insulators generating a compact circuit based representation that is compatible with the rest of the PDK. RF designers will now be able to accurately model parasitic physical effects that impact the integration of critical analog and RF functions in complex electronic systems for next generation cellular and Wi-Fi communication chips. TowerJazz's CS18 PDKs is offered with SiPEX™ already integrated.

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"We are excited to be entering into this partnership with CWS. By integrating SiPEX into our CS18 process design kits, our customers will now have the tools to optimize their designs to the best capabilities offered by our RF SOI processes. This unique solution analyzes coupling within critical analog functions, while also allowing for simulation of cross-talk across the chip," said Ori Gazlur, vice president of VLSI design center and design enablement at TowerJazz.

SiPEX™ helps the RF silicon-on-insulator (SOI) design community improve their RF designs by addressing RF switches. This will soon be followed by low-noise amplifiers (LNA) and power amplifier (PA) designs that benefit from a technology breakthrough that results in a 10 decibel (dB) improvement.

"This is great news for the RF design community. TowerJazz will provide our customers with a dramatic enhancement," said Brieuc Turluche, chairman of the board of directors and chief executive officer of CWS. "The integration of SiPEX into TowerJazz's CS18 PDK is a first step that will enable RF designers design switches suitable for up-link carrier aggregation. Soon we will provide a more generic solution to improve the performance of other RF front-end module circuits like power and low-noise amplifiers. Taken together, these enhancements will help RF designers create high-performing next generation communication chips."

Availability

SiPEX is available in the current release of TowerJazz's CS18 PDK.

About CWS

CWS is the leading provider of parasitic extraction and activity modeling tools for system-level interference analysis of complex designs incorporating RF and analog blocks, targeting SOI applications or advanced bulk process nodes including 28nm and below. CWS unique harmonic analysis approach allows for controlling and managing noise issues throughout the design cycle from components, to packages, up to and including board design. Wrapped in 'easy-to-deploy' software bundle, WaveIntegrity™ is used by chip architects and designers to drive the chip design floorplanning and by package and PCB designers to integrate the noise-related design constraints in the final chip operational environment. Founded in 2003, CWS' offices are located in Paris, Grenoble, France and San Jose, USA. More information about the company, its products, and services is available at www.cwseda.com.

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