



## ***PRESS RELEASE***

---25<sup>th</sup> February, 2013

### **WaveIntegrity™ from CWS Selected By STMicroelectronics to Provide Critical Noise Analysis And Reduce Power Pin Requirements in Bulk CMOS and FD-SOI SoCs**

#### **Users Reduce Risk in Three Main Areas, Providing Verification Previously Impossible**

**Moirans, France., February 25th, 2013** – Coupling Wave Solutions, S.A. (CWS), a leader in solutions for noise analysis in complex A/MS SoC designs, today announced that STMicroelectronics has adopted the WaveIntegrity™ analysis tools to remove risk caused by on-chip, package and PCB parasitics. Following multiple evaluations, covering use for both CMOS and FD-SOI processes, a leading contender for next-generation Low-Power Products fabrication, STMicroelectronics is deploying WaveIntegrity™ across groups designing complex IP, Digital Convergence Products and Automotive devices.

CWS has worked closely with STMicroelectronics to ensure its teams have full visibility of potential noise issues in their IP and SoC designs. As a result, STMicroelectronics users of WaveIntegrity™ benefit from a proven, flexible and highly differentiated verification solution.

“Minimizing power while maximizing performance and securing functionality is driving STMicroelectronics’s adoption of new tools and methodologies. The comprehensive CWS noise analysis solution has enabled our teams to successfully identify and avoid significant noise issues in mixed-signal SOCs,” said Philippe Magarshack, STMicroelectronics Executive Vice President. “The close and ongoing cooperation with CWS is helping our teams achieve success with next-generation designs incorporating advanced analog and digital IPs, across a range of processes, including our latest advances in FD-SOI.”

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#### **S.A. Coupling Wave Solutions (CWS)**

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STMicroelectronics has used WaveIntegrity™ to analyze 28nm FD-SOI SOCs, minimize power-supply bumps and pin count, analyze digital noise on I/Os in 55nm CMOS automotive designs, and ensure mixed digital and RF ICs are clean of noise issues, at 40nm and below. This has required the development of methodologies appropriate to the specific requirements of each type of design, as well as the wider adoption of more “standard” techniques enabled by WaveIntegrity™.

“The complexity and frequency of SoC designs increase year-on-year, together with increasingly stringent power requirements. Successfully verifying the noise characteristics of the SoCs, the package they are placed in and the PCBs they are inserted on, has become an increasingly difficult challenge: applying “rules of thumb” is no longer adequate. The capabilities of WaveIntegrity™ provide and support such analysis, and enable verification previously considered impractical by other means,” commented Brieuc Turluche, president and CEO of CWS. “With multiple teams contributing to each design it is essential that noise analysis is both easy and rapid to implement at each stage.”

To learn more visit [www.cwseda.com](http://www.cwseda.com)

#### **About CWS**

CWS enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use CWS software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in 196C, Rue du Rocher de LORZIER, F-38430, Moirans, France. More information about the company, its products, and services is available at [www.cwseda.com](http://www.cwseda.com).

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